M24512-x
M24256-Bx

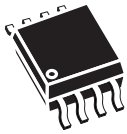
512 Kbit and 256 Kbit serial I²C bus EEPROM with three Chip Enable lines

Features

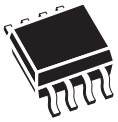
- Supports the I²C bus 100 kHz Standard-mode, 400 kHz Fast-mode and 1 MHz Fast-mode Plus
- Supply voltage ranges:
  - 1.7 V to 5.5 V (M24256-BF)
  - 1.8 V to 5.5 V (M24xxx-R)
  - 2.5 V to 5.5 V (M24xxx-W)
- Write Control input
- Byte and Page Write
- Random and sequential read modes
- Self-timed programming cycle
- Automatic address incrementing
- Enhanced ESD/latch-up protection
- More than 1 000 000 write cycles
- More than 40-year data retention
- Packages
  - ECOPACK® (RoHS compliant)

Table 1. Device summary

Reference	Part numbers
M24512-x	M24512-R, M24512-HR, M24512-W
M24256-Bx	M24256-BF, M24256-BR, M24256-BHR, M24256-BW

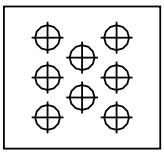


SO8 (MW)
208 mils width



SO8 (MN)
150 mils width

TSSOP8 (DW)



WLCSP (CS)

1 Description

The M24512-W, M24512-R, M24512-HR, M24256-BF, M24256-BW, M24256-BR and M24256-BHR devices are I^2C-compatible electrically erasable programmable memories (EEPROM). They are organized as 64 Kb × 8 bits and 32 Kb × 8 bits, respectively.

I^2C uses a two-wire serial interface, comprising a bidirectional data line and a clock line. The devices carry a built-in 4-bit Device Type Identifier code (1010) in accordance with the I^2C bus definition.

The device behaves as a slave in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a device select code and Read/$\overline{\text{Write}}$ bit ($\overline{\text{RW}}$) (as described in *Table 3*), terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

Figure 1. Logic diagram

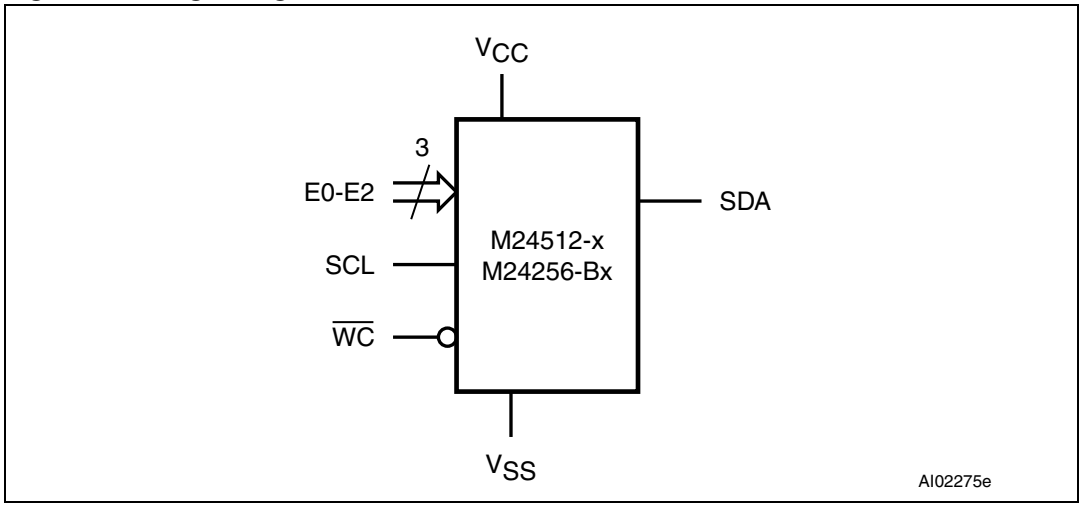


Table 2. Signal names

Signal name	Function	Direction
E0, E1, E2	Chip Enable	Inputs
SDA	Serial Data	I/O
SCL	Serial Clock	Input
$\overline{\text{WC}}$	Write Control	Input
V_{CC}	Supply voltage	
V_{SS}	Ground	

4 Initial delivery state

The device is delivered with all bits in the memory array set to 1 (each byte contains FFh).

5 Maximum rating

Stressing the device outside the ratings listed in *Table 7* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 7. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient operating temperature	–40	130	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	See note (1)		°C
V_{IO}	Input or output range	–0.50	V_{CC} + 0.6	V
V_{CC}	Supply voltage	–0.50	6.5	V
V_{ESD}	Electrostatic discharge voltage (human body model) (2)	–4000	4000	V

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS) 2002/95/EC.
2. AEC-Q100-002 (compliant with JEDEC Std JESD22-A114, C1 = 100 pF, R1 = 1500 Ω, R2 = 500 Ω)

6 DC and AC parameters

This section summarizes the operating and measurement conditions, and the dc and ac characteristics of the device. The parameters in the DC and AC characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 8. Operating conditions (M24xxx-W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature (device grade 6)	–40	85	°C
	Ambient operating temperature (device grade 3)	–40	125	°C

Table 9. Operating conditions (M24xxx-R and M24xxx-HR)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 10. Operating conditions (M24256-BF)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.7	5.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 11. AC test measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	100		pF
	Input rise and fall times		50	ns
	Input levels	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input and output timing reference levels	$0.3V_{CC}$ to $0.7V_{CC}$		V

Figure 12. AC test measurement I/O waveform

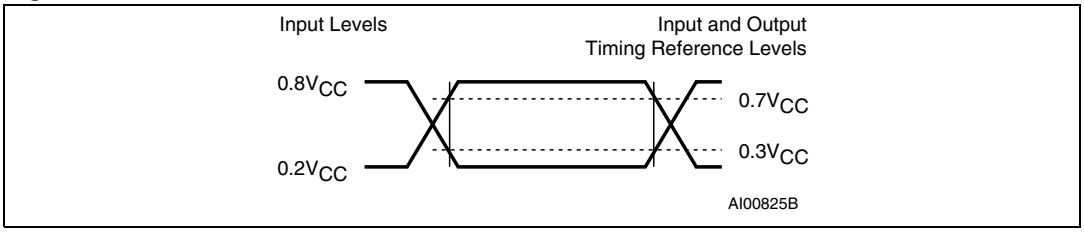


Table 12. Input parameters

Symbol	Parameter[1]	Test condition	Min.	Max.	Unit
C_{IN}	Input capacitance (SDA)			8	pF
C_{IN}	Input capacitance (other pins)			6	pF
Z_L[2]	Input impedance (E2, E1, E0, $\overline{WC}$)	$V_{IN} < 0.3V_{CC}$	30		kΩ
Z_H[2]	Input impedance (E2, E1, E0, $\overline{WC}$)	$V_{IN} > 0.7V_{CC}$	500		kΩ

1. Sampled only, not 100% tested.
2. E2,E1,E0: Input impedance when the memory is selected (after a Start condition).

Table 13. DC characteristics (M24xxx-W)

Symbol	Parameter	Test conditions (see *Table 8* and *Table 11*)		Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA, E0, E1, E2)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode			± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}			± 2	µA
I_{CC}	Supply current (Read)	V_{CC} = 2.5 V, f_c = 400 kHz (rise/fall time < 50 ns)			1	mA
		V_{CC} = 5.5 V, f_c = 400 kHz (rise/fall time < 50 ns)			2	mA
I_{CC0}	Supply current (Write)	During t_W, 2.5 V < V_{CC} < 5.5 V			5[1]	mA
I_{CC1}	Standby supply current	Device not selected[2], $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5 V	Device grade 3		5	µA
			Device grade 6		2	
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5.5 V			5	µA
V_{IL}	Input low voltage (SCL, SDA, $\overline{WC}$)			–0.45	$0.3V_{CC}$	V
V_{IH}	Input high voltage (SCL, SDA, $\overline{WC}$)			$0.7V_{CC}$	V_{CC}+0.6	V
V_{OL}	Output low voltage	I_{OL} = 2.1 mA, V_{CC} = 2.5 V			0.4	V

1. Characterized value, not tested in production.
2. The device is not selected after power-up, after a READ command (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a WRITE command).

Table 14. DC characteristics (M24xxx-R and M24xxx-HR)

Symbol	Parameter	Test conditions (in addition to those in *Table 9*)	Min.	Max.	Unit
I_{LI}	Input leakage current (E1, E2, SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode		± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	V_{CC} = 1.8 V, f_c= 400 kHz (rise/fall time < 50 ns)		0.8	mA
		V_{CC} = 2.5 V, f_c= 400 kHz (rise/fall time < 50 ns)		1	mA
		V_{CC} = 5.0 V, f_c= 400 kHz (rise/fall time < 50 ns)		2	mA
		1.8 V < V_{CC} < 5.5 V, f_c= 1 MHz(1) (rise/fall time < 50 ns)		2.5	mA
I_{CC0}	Supply current (Write)	During t_W, 1.8 V < V_{CC} < 5.5 V		5(2)	mA
I_{CC1}	Standby supply current	Device not selected(3), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.8 V		1	µA
		Device not selected(3), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5 V		2	µA
		Device not selected(3), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5.5 V		3	µA
V_{IL}	Input low voltage (SCL, SDA, $\overline{WC}$)	1.8 V ≤ V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
		2.5 V ≤ V_{CC} ≤5.5 V	–0.45	0.3 V_{CC}	
V_{IH}	Input high voltage (SCL, SDA, $\overline{WC}$)	1.8 V ≤ V_{CC} < 2.5 V	0.75V_{CC}	V_{CC}+1	V
		2.5 V ≤ V_{CC} ≤ 5.5 V	0.7V_{CC}	V_{CC}+1	
V_{OL}	Output low voltage	I_{OL} = 1 mA, V_{CC} = 1.8 V		0.2	V
		I_{OL} = 2.1 mA, V_{CC} = 2.5 V		0.4	V
		I_{OL} = 3.0 mA, V_{CC} = 5.5 V		0.4	V

1. Only for M24xxx-HR6.
2. Characterized value, not tested in production.
3. The device is not selected after power-up, after a READ command (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a WRITE command).

Table 15. DC characteristics (M24256-BF)(1)

Symbol	Parameter	Test condition (in addition to those in *Table 9*)	Min.	Max.	Unit
I_{LI}	Input leakage current (E1, E2, SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode		± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	V_{CC} = 1.7 V, f_c= 400 kHz (rise/fall time < 50 ns)		0.8	mA
		V_{CC} = 2.5 V, f_c= 400 kHz (rise/fall time < 50 ns)		1	mA
		V_{CC} = 5.0 V, f_c= 400 kHz (rise/fall time < 50 ns)		2	mA
		1.7 V < V_{CC} < 5.5 V, f_c= 1 MHz(2) (rise/fall time < 50 ns)		2.5	mA
I_{CC0}	Supply current (Write)	During t_W, 1.7 V < V_{CC} < 5.5 V		5(3)	mA
I_{CC1}	Standby supply current	Device not selected(4), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.7 V		1	µA
		Device not selected(4), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5 V		2	µA
		Device not selected(4), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5.5 V		3	µA
V_{IL}	Input low voltage (SCL, SDA, $\overline{WC}$)	1.7 V ≤ V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
		2.5 V ≤ V_{CC} ≤ 5.5 V	–0.45	0.3 V_{CC}	
V_{IH}	Input high voltage (SCL, SDA, $\overline{WC}$)	1.7 V ≤ V_{CC} < 2.5 V	0.75V_{CC}	V_{CC}+1	V
		2.5 V ≤ V_{CC} ≤ 5.5 V	0.7V_{CC}	V_{CC}+1	
V_{OL}	Output low voltage	I_{OL} = 1 mA, V_{CC} = 1.7 V		0.2	V
		I_{OL} = 2.1 mA, V_{CC} = 2.5 V		0.4	V
		I_{OL} = 3.0 mA, V_{CC} = 5.5 V		0.4	V

1. Preliminary data.
2. Only for M24xxx-HR6.
3. Characterized value, not tested in production.
4. The device is not selected after power-up, after a READ command (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a WRITE command).

Table 16. AC characteristics (M24xxx-W, M24xxx-R, M24256-BF see *Table 8*, *Table 9* *Table 10* and *Table 11*)

Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency		400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	600		ns
t_{CLCH}	t_{LOW}	Clock pulse width low	1300		ns
t_{DL1DL2}(1)	t_F	SDA (out) fall time	20	100	ns
t_{XH1XH2}(2)	t_R	Input signal rise time	20	300	ns
t_{XL1XL2}(2)	t_F	Input signal fall time	20	300	ns
t_{DXCX}	$t_{SU:DAT}$	Data in set up time	100		ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0		ns
t_{CLQX}	t_{DH}	Data out hold time	200		ns
t_{CLQV}(3)	t_{AA}	Clock low to next data valid (access time)	200	900	ns
t_{CHDX}(4)	$t_{SU:STA}$	Start condition set up time	600		ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	600		ns
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	600		ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	1300		ns
t_W	t_{WR}	Write time		5	ms
t_{NS}		Pulse width ignored (input filter on SCL and SDA) - single glitch		100	ns

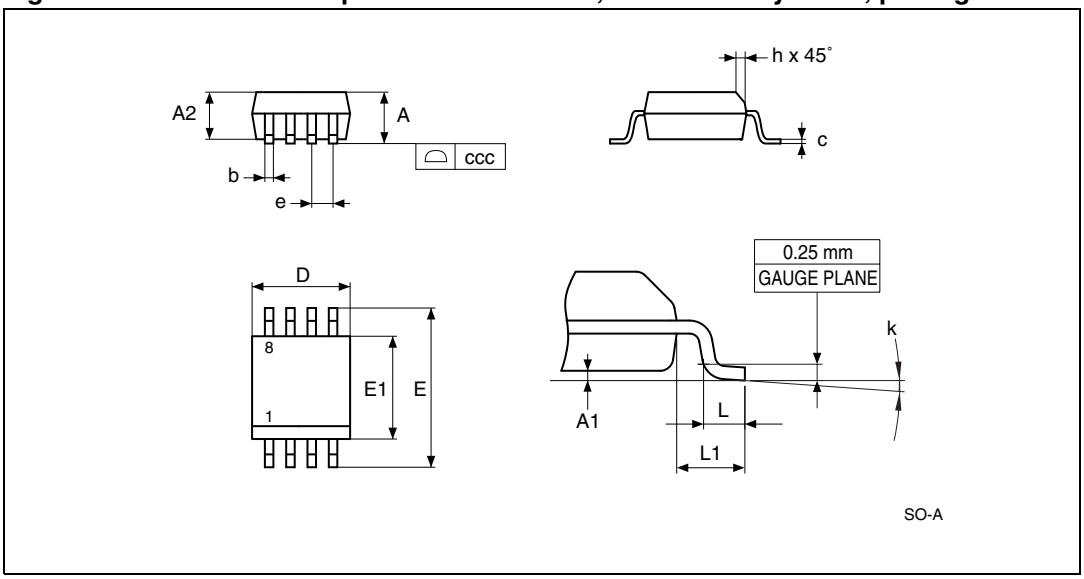
1. Sampled only, not 100% tested.
2. Values recommended by I²C-bus/Fast-Mode specification.
3. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
4. For a re-Start condition, or following a Write cycle.

Table 17. 1 MHz AC characteristics (M24xxx-HR, see *Table 9* and *Table 11*)

Test conditions specified in *Table 9*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCL}	Clock frequency	0	1	MHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	300	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	400	-	ns
t_{XH1XH2}(1)	t_R	Input signal rise time	20	300	ns
t_{XL1XL2}(1)	t_F	Input signal fall time	20	300	ns
t_{DL1DL2}(2)	t_F	SDA (out) fall time	20	100	ns
t_{DXCX}	$t_{SU:DAT}$	Data in setup time	80	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX}	t_{DH}	Data out hold time	50	-	ns
t_{CLQV}(3)(4)	t_{AA}	Clock low to next data valid (access time)	50	500	ns
t_{CHDX}(5)	$t_{SU:STA}$	Start condition setup time	250	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	250	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition setup time	250	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	500	-	ns
t_W	t_{WR}	Write time	-	5	ms
t_{NS}(2)		Pulse width ignored (input filter on SCL and SDA)	-	50	ns

1. Values recommended by the I²C-bus Fast-Mode specification.
2. Characterized only, not tested in production.
3. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
4. t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach $0.8V_{CC}$, assuming that the $R_{bus} \times C_{bus}$ time constant is less than 150 ns (as specified in *Figure 5*).
5. For a reStart condition, or following a Write cycle.

Figure 15. SO8N – 8-lead plastic small outline, 150 mils body width, package outline



1. Drawing is not to scale.

Table 19. SO8N – 8-lead plastic small outline, 150 mils body width, package mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.0689
A1		0.1	0.25		0.0039	0.0098
A2		1.25			0.0492	
b		0.28	0.48		0.011	0.0189
c		0.17	0.23		0.0067	0.0091
ccc			0.1			0.0039
D	4.9	4.8	5	0.1929	0.189	0.1969
E	6	5.8	6.2	0.2362	0.2283	0.2441
E1	3.9	3.8	4	0.1535	0.1496	0.1575
e	1.27	-	-	0.05	-	-
h		0.25	0.5		0.0098	0.0197
k		0°	8°		0°	8°
L		0.4	1.27		0.0157	0.05
L1	1.04			0.0409		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

8 Part numbering

Table 22. Ordering information scheme

Example: M24512– H W MW 6 T P /AB

Device type

M24 = I^2C serial access EEPROM

Device function

512– = 512 Kbit (64 Kb × 8)

256–B = 256 Kbit (32 Kb × 8)

Clock frequency

Blank: f_C max = 400 kHz

H: f_C max = 1 MHz

Operating voltage

W = V_{CC} = 2.5 to 5.5 V

R = V_{CC} = 1.8 to 5.5 V

F = V_{CC} = 1.7 to 5.5 V

Package

MW = SO8 (208 mils width)

MN = SO8 (150 mils body width)

DW = TSSOP8

CS = WLCSP

Device grade

6 = Industrial temperature range, –40 to 85 °C. Device tested with standard test flow

3 = Automotive: device tested with high reliability certified flow(1) over –40 to 125 °C

Option

blank = standard packing

T = tape and reel packing

Plating technology

P or G = ECOPACK® (RoHS compliant)

Process(2)

/A = F8L in CSP package

/AB = F8L for device grade 3

1. ST strongly recommends the use of the Automotive Grade devices for use in an automotive environment. The High Reliability Certified Flow (HRCF) is described in the quality note QNEE9801. Please ask your nearest ST sales office for a copy.
2. Used only for device grade 3 and WLCSP packages.